

## RF performance tradeoffs of SiGe HBT fabricated by reduced pressure chemical vapor deposition

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**Abstract** — In this paper we developed high cutoff frequency and low noise SiGe HBT devices using reduced pressure chemical vapor deposition (RPCVD) process of low cost and high throughput. In addition the RPCVD can alleviate large thermal variation even on a single wafer as occurs in ultra-high vacuum chemical vapor deposition (UHVCVD) process. We also adopted the cheap localized oxidation of silicon (LOCOS) instead of shallow trench for the isolation of terminals to reduce the parasitic from linkage at RF arena. The cutoff frequency and maximum oscillation frequency of SiGe HBT having the emitter size of  $1 \times 2.5 \mu\text{m}^2$  were 48 and 62 GHz, respectively. With the tradeoff of base profile and adopting finger-type base structure the measured minimum noise figure of 1.5 dB and associated gain of 16 dB at 1.5 GHz consuming the collector current of 3.1 mA were also observed in the low noise device. Limitation of noise performance related with this process was also discussed.

fabrication cost. Thus the self-aligned structure was used in this paper. In some advanced processes chemical-mechanical polishing (CMP) and shallow trench are used, which can reduce these parasitics effectively to increase device performance [2]. But these processes are different from that of widely used in conventional CMOS process and, moreover, need additional development cost to adopt. Since the widely prevailed technology has economic merits, we used the traditional LOCOS process in spite of suffering RF performance limitation.

Our purpose of this paper is to verify the low cost implementation of SiGe HBT process having high frequency performance and low noise property by the trade-off of RF performances without introducing expensive process technologies.

### I. INTRODUCTION

Today RF front-end market issues at device fabrication level are characterized by three factors: 1) low noise with high gain at low current consumption, 2) high linearity without compromising, and 3) low cost for fabrication, the first two of which are crucial to the receiver design relieving from various problems at the front-end and base-band design, and the last of which is the result of overwhelming growth of wireless electronics market. The fabrication process should maintain the first two facts while reducing cost as possible. Especially because low noise properties at low power consumption make possible portable devices with smaller batteries, i.e. lighter products, the first factor is of prime importance in the portable market. From this point of view the economic SiGe HBT by RPCVD having properties of low cost, low noise, high gain and high linearity at low power consumption gives another solution to the current RF front-end market.

In the early time non-self aligned SiGe HBT by RPCVD was developed [1] in which the extrinsic base resistance and series emitter resistance can be reduced, enhancing

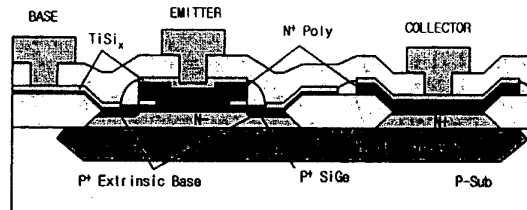


Fig. 1. Schematics of the SiGe HBT fabricated

### II. DEVICE FABRICATION

The standard SiGe HBT is shown in Fig. 1. A junction and LOCOS isolation were used to isolate devices and device terminals respectively. The thickness of collector was 8000 Å on the thick and highly doped sub-collector. The base epitaxial layer was grown by RPCVD. Standard base profile was shown in Fig. 2(a). To investigate the effect of thick base on noise properties, the base profile was designed as shown in Fig. 2(b). In the standard base profile the total Ge thickness was 400 Å with the rectangular layer of Boron (150 Å). The base growth was followed by the oxidation (O<sub>2</sub>) that is critical to

the intrinsic base-emitter junction. The C54-TiSi<sub>2</sub> was obtained by rapid thermal anneal at 850 °C for 30 second with no harm to the base profile.

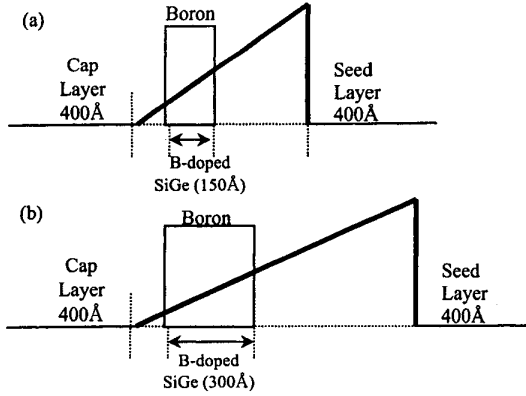


Fig. 2. Base profile used; a) the standard base profile, b) the thick base profile

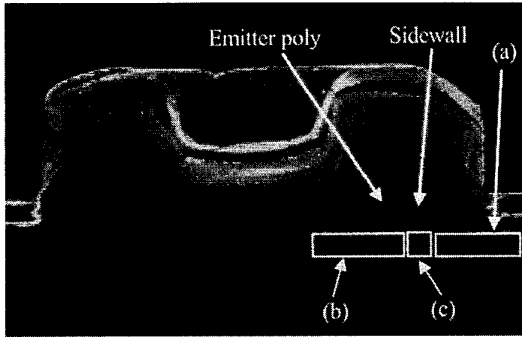


Fig. 3. Three parts that affect the extrinsic base resistance

Fig. 3 shows three parts that is related to the extrinsic base resistance. The self-aligned Ti-silicidation was applied at (a) but at (b) and (c) because of the emitter poly and the emitter sidewall, respectively. The region (b) and (c) were known to be the bottleneck in decreasing extrinsic base resistance. So the shallow trench with CMP process is normally used and the emitter dimension is scaled down. Whenever the LOCOS was adopted with the thin base, however, the Ti-silicidation at (a) could not be achieved to the sufficient extent resulting in relatively higher resistance than at (b) and (c). Thus the base layer was grown thick as an alternative of the enhancement of Ti-silicidation as shown in Fig. 2(b). That will positively affect the extrinsic base and noise property. Beside the thick base the multi-finger structure would assist the

extrinsic base resistance to be reduced in spite of a little increases of parasitic capacitance at the extrinsic base-emitter and/or base-collector junctions.

We measured and analyzed the HBT's having the emitter size of  $1 \times 2.5 \mu\text{m}^2$  (device-A) and ten fingers of  $1 \times 6 \mu\text{m}^2$  (device-B) in both of the standard SiGe HBT process and the thick base profile process.

### III. RESULTS

#### A. DC and AC characteristics

Using Agilent parameter analyzer 4156B and Cascade probe station DC characteristics were measured on wafer. IV curves and gummel plots are shown in Fig. 4 and Fig. 5, respectively. In device-A, the peak DC current gains of standard profile and thick base profile were 700 and 270 at the collector current of 0.41 mA and 0.56 mA, respectively. The current gains were nearly flat over a wide range of collector current. Collector-emitter breakdown voltages of standard process and thick base process were 4.6V and 4.2V, respectively. Early voltages of all devices were over 50 V enabling high output impedance and good small signal performance.

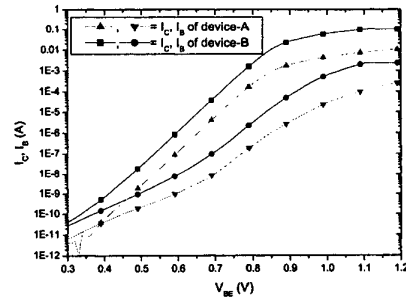


Fig. 4. Gummel plots of device A and B in the standard profile

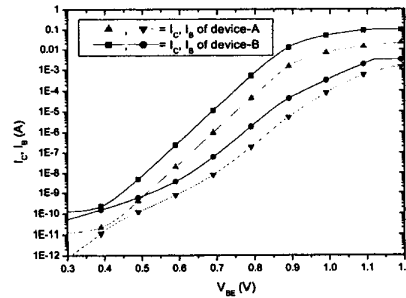


Fig. 5. Gummel plots of device A and B in the thick base profile

Using Agilent DC modular source 4142B and network analyzer 8510C the scattering parameters were measured. De-embedding procedure followed scattering parameter measurement to eliminate the pad and ground line parasitics [3]. From the de-embedded result we calculated the cutoff frequency for the devices in standard process and thick base process as shown in Fig. 6 and Fig. 7, respectively according to the current density, i.e. the emitter current in a unit emitter size. The maximum cutoff frequencies of device-A and -B in standard process were 48 GHz and 31 GHz, and those in thick base process were 34 GHz and 28 GHz. In the thick base profile the cutoff frequency of the single finger device, device-A was severely decreased, since the base transit time was increased by thicker base, while that of the multi-finger device, device-B was nearly same, because the base transit time of device-B in the standard profile was not limited by base thickness but the parasitics such like extrinsic base-emitter capacitance. The maximum oscillation frequencies of device-A in the standard and thick base process were also measured as about 62 GHz and 41 GHz.

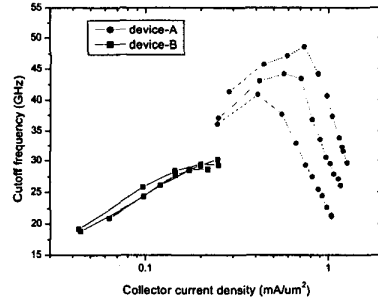


Fig. 6. Cutoff frequency of device A and B in the standard profile at the collector-emitter voltage of 1, 2 and 3 V

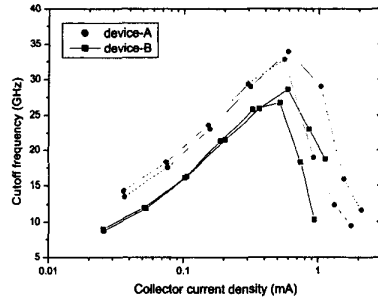


Fig. 7. Cutoff frequency of device A and B in the thick base profile at the collector-emitter voltage of 1 and 2 V

The extrinsic base and emitter resistances can be directly extracted from the de-embedded result using semi-circle diagram method [4]. From this method, the extrinsic base and emitter resistances of device-B in the standard profile were 15  $\Omega$  and 1.1  $\Omega$ , and those of device-B in the thick base profile were 5  $\Omega$  and 0.9  $\Omega$ , respectively.

### B. Noise characteristics

Noise parameters were measured using Agilent 8970B noise figure measurement system with the ATN NP5 automatic tuners which changing input impedance of the device under test, enabling faster measurement than a mechanical tuner. But this measurement includes calibration process that may affect a detrimental effect on the measured results. Even though the several methods are provided to alleviate these problems including fitting algorithms, reliable results can be gained by repeated measurements and result inspections.

After repeated and cautious noise measurement, we found that device-B in thick base process has the minimum noise figures of 0.5 dB and 1.5 dB at 900 MHz and 1.5 GHz, respectively, while device-B in the standard process has over 3 dB. These minimum noise figures were obtained at the collector current of 0.5 mA and 3.1 mA, respectively, which is quite lower power consumption compared with the result of general CMOS process. Moreover these associated gains, the maximum available gains with the source matched to the noise minimum points, were 17 dB and 16 dB, respectively, even at the low current consumption. The minimum noise figure and the associated gain of device-B in thick base process are shown in detail at Fig. 7 and Fig. 8 according to collector current and frequency, respectively.

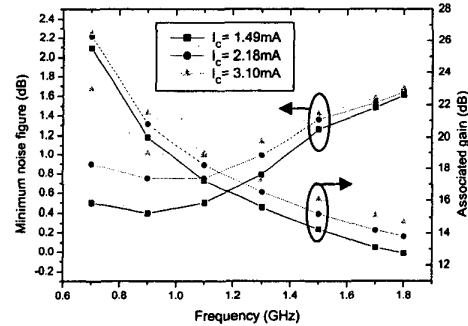


Fig. 7. The minimum noise figure and the associated gain versus frequency of the device-B in the thick base profile

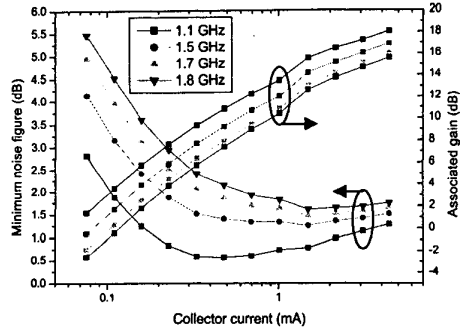


Fig. 8. The minimum noise figure and the associated gain versus the collector current of the device-B in the thick base profile

#### IV. DISCUSSION

In standard process the extrinsic emitter resistance was quite small, while the extrinsic base resistance was not small and must be decreased to enhance noise performance. In thick base profile the extrinsic base resistance was decreased significantly sacrificing the cutoff frequency. From the result of the extracted extrinsic base resistance, it explains that the resistance reduction by multi-finger structure reaches the lower limit of the resistance. It also means that the region where Ti-silicidation is applied is more important to noise performance than the area where Ti-silicidation is not applied in the current process condition. This is because the distance where Ti-silicidation is applied is relatively long ranging from the base contact to the emitter sidewall, and the base thickness is insufficient to get low resistance by Ti-silicidation. Consequently, changing base profile, we can make a trade-off between low noise and high performance of SiGe HBT. So the RF front-end products developed by this approach can be cheaper while maintaining the RF and noise performance.

Additionally, in spite that multi-finger type device can decrease the extrinsic base resistance to enhance the minimum noise figure, the increased base-collector feedback capacitance makes the device unstable. Moreover the high gain LNA that located after the

measured device in the noise measurement system deteriorates the stable condition of the measured device and disturbs the noise measurement. Therefore low noise devices need to be stable as possible for the proper device characterization. To realize low noise devices without such a problem, emitter width should be scaled down and parasitics maintained to have low values. However these conditions increase the cost of the SiGe HBT process. For the huge market and increased pressure of low fabrication cost, the results with these limits can be adopted in low price wireless products.

#### V. CONCLUSION

SiGe HBT's using low price process featuring RPCVD and the traditional LOCOS process were analyzed. In the standard profile the peaks of measured cutoff and maximum oscillation frequencies were 48 GHz and 62 GHz, respectively, at the emitter size of  $1 \times 2.5 \mu\text{m}^2$ . In the thick base profile the device of ten fingers with the emitter size of  $1 \times 6 \mu\text{m}^2$  had a minimum noise figure and an associated gain of 1.5 dB and 16 dB, respectively, at 1.5 GHz with the collector current of 3.1 mA. Without an expensive process introduced, it was verified that a trade-off between noise and high performance could be possible.

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